Abstract—This article presents the design and realization of a two stage dual band (1.575 GHz and 2.680 GHz) Wilkinson power divider on silicon substrate using microstrip technology. The design incorporates compact open stub in serpentine shape. Step impedance resonator (SIR) in T-shaped stub is incorporated to provide additional degree of freedom. The measured performance shows insertion loss variation of ±0.4 dB (max.), return loss better than 15 dB and isolation greater than 13 dB at both the frequency bands and the results are in close agreement with the simulation.

Index Terms—dual band, high resistive silicon, microstrip line, T-shaped stub, wilkinson power divider.

I. INTRODUCTION

Wilkinson power dividers find wide usage in antenna feeds because of good isolation property in comparison with conventional T-splitters, resistive dividers and quarter-wave couplers. Conventional Wilkinson divider operates at a single frequency due to incorporation of quarter wave transmission line resulting in narrow bandwidth [1]. Modern communication systems demand compact multi-band operations with enhanced performance. Inherent losses in planar technology restrict the operation to at most three bands in microstrip technology without modifications in ground plane and addition of external elements [2]. Dual band power dividers operate at frequencies such that their frequency ratio lies between 2.00 to 2.75 [3]. The small dual-frequency transformer in two sections showed poor output return loss and port isolation [4,5]. The present topology, an extension of work carried by Cheng & Wong [3], overcomes the limitation imposed on the permittivity of the medium by meandering and incorporating T-shaped open stub at the stub end. An extra degree of freedom is facilitated with incorporation of Step Impedance Resonator (SIR) approach [6], which adjusts the frequency response while implementing on various substrates. This paper presents the design and development of 1:4 divider having centre frequencies at 1.575 GHz (L-band) and 2.680 GHz (S-band) for GPS/MSS applications. This approach is validated by carrying out simulation study using electromagnetic tool on both Glass and silicon substrates. The structure is realized on high resistivity silicon and measured performance is in close agreement with simulation.

II. DESIGN METHODOLOGY

The standard single-band Wilkinson power divider consists of two quarter-wavelength branch-lines with impedance √2Z₀ and an isolation resistor of 2Z₀, where Z₀ is the characteristic impedance of the transmission line (Z₀=50Ω).

Kamaljeet Singh is with the Semi-Conductor Laboratory, Near Chandigarh, India 0172-2237401-10; e-mail: kamaljs@ scl.gov.in
Ayan Karamakar is with the Semi-Conductor Laboratory, Near Chandigarh, India 0172-2237401-10; e-mail: ayanns@ scl.gov.in
K Nagachenchaiah is with the Semi-Conductor Laboratory, Near Chandigarh, India 0172-2237401-10; e-mail: kamaljs@ scl.gov.in

The dual band topology is modified as proposed by Cheng and Wong [3] by incorporating two cascaded quarter wave line sections with different impedances along with short/open ended stub between the cross-junction as shown in Fig.1(b).

Numerically, the value of Zₐ, Z₋, Zₛ and Zₒ are computed using Eqn. (1).

\[
\begin{align*}
Z_A &= \sqrt{2Z_0} \tan \frac{\Pi \varepsilon}{2} \\
Z_B &= \sqrt{2Z_0} \cot \frac{\Pi \varepsilon}{2} \\
Z_S &= \frac{Z_0 \tan \Pi \varepsilon}{\sqrt{2}} \tan \frac{\Pi \varepsilon}{2} \\
Z_O &= \frac{Z_0 \tan^2 \Pi \varepsilon}{\sqrt{2}} \tan \frac{\Pi \varepsilon}{2}
\end{align*}
\]

Where, ε and f₀ are given by,

\[
\varepsilon = \frac{f_2 - f_1}{f_2 + 1} \quad \text{and} \quad f_0 = \frac{f_1 + f_2}{2}
\]
where, \( f_1 \) and \( f_2 \) are the desired frequencies; \( Z_{SC} \) and \( Z_{OC} \) are the short and open-circuited stub impedances respectively. Instead of short-circuited stub, the structure incorporates open-end stub at the cost of increased line length, to avoid fabrication intricacies and introduction of parasitic inductance. The meandered open stub makes the circuit compact and also offers additional degree of tuning because of mutual coupling between the adjacent lines as shown in Fig. 2(a). By varying the coupling distance, a good input/output return loss as well as isolation can be achieved. T-shaped stub with SIR approach in the end facilitates additional variability for the placement of transmission zeros [6]. The improvement in return loss with the inclusion of SIR stub is shown in Table 1 for various substrates.

### Table 1: Effect of T-Stub

<table>
<thead>
<tr>
<th>Substrate</th>
<th>( \varepsilon_r )</th>
<th>tan ( \delta )@3 GHz</th>
<th>Return Loss (dB) without T-stub</th>
<th>Return Loss (dB) with T-stub</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT/Duroid 6002</td>
<td>2.94</td>
<td>0.0012</td>
<td>-4.10</td>
<td>-5.95</td>
</tr>
<tr>
<td>FR-4</td>
<td>4.80</td>
<td>0.0220</td>
<td>-3.95</td>
<td>-7.85</td>
</tr>
<tr>
<td>Soda-glass</td>
<td>4.82</td>
<td>0.0054</td>
<td>-3.92</td>
<td>-7.95</td>
</tr>
<tr>
<td>Alumina</td>
<td>9.80</td>
<td>0.0001</td>
<td>-10.59</td>
<td>-11.75</td>
</tr>
<tr>
<td>Silicon</td>
<td>11.8</td>
<td>0.0010</td>
<td>-12.68</td>
<td>-14.28</td>
</tr>
<tr>
<td>GaAs</td>
<td>12.8</td>
<td>0.0016</td>
<td>-13.32</td>
<td>-16.58</td>
</tr>
</tbody>
</table>

MOM & FEM based analysis [7] is carried out to optimize the structure on both silicon and glass substrates.

Based on the closed-form expressions given by eqn.(1) and further optimization, values of \( Z_A, Z_B \) and \( Z_{SC} \) are found out as \( 82\Omega, 131\Omega \) and \( 48\Omega \), respectively for silicon (\( \varepsilon_r =11.8 \)), whereas for glass (\( \varepsilon_r = 4.82 \)) substrate the optimized values are \( 85.36\Omega, 92.16\Omega \) and \( 70.18\Omega \), respectively. Pad dimension 1.8 mm \( \times \) 1 mm along with gap of 1.5 mm has been incorporated for mounting the isolation resistor of \( 2Z_B \) between two output ports. Layout area for silicon is 28 mm \( \times \) 56 mm which is 2.5 times lesser compared to glass (47 mm \( \times \) 87 mm) due to difference in permittivity values. 1:2 divider is cascaded with two similar structures at the output ports resulting in 1:4 divider as shown in Fig 3. Open stub length is further increased in the overall structure and optimized to achieve the desired response.

![Fig. 2. Layout of the proposed first stage power divider](image)

![Fig. 3. Layout of the proposed four port (1:4) power divider on Silicon](image)

Table 2 shows comparative performance study of power divider on glass and silicon substrate using simulation data.

### Table II

<table>
<thead>
<tr>
<th>Type of Substrate</th>
<th>Frequency(GHz)</th>
<th>Input Return Loss(dB)</th>
<th>Output Return Loss(dB)</th>
<th>Insertion Loss(dB)</th>
<th>Output Port Isolation(dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass ( (\varepsilon_r = -1.8) )</td>
<td>1.575</td>
<td>-14.59</td>
<td>-12.54</td>
<td>-6.528</td>
<td>-13.021</td>
</tr>
<tr>
<td></td>
<td>2.680</td>
<td>-27.194</td>
<td>-21.237</td>
<td>-6.179</td>
<td>-134.21</td>
</tr>
</tbody>
</table>

As can be seen the losses are higher, by about 0.3 dB on glass substrate, due to higher substrate losses in glass medium.

### III. Fabrication and Measured Results

Fabrication of the structure is carried out using standard CMOS process on high resistivity (\( \rho > 8 \text{ K}\Omega\text{-cm} \)) 6" wafer of 675 \( \mu \text{m} \) thicknesses. 3 \( \mu \text{m} \) PECVD oxide has been deposited as a buffer layer. Metallization is done using electron beam evaporation and standard wet chemistry is employed for etching purpose. The minimum dimension used in the fabricated structure is 5\( \mu \text{m} \). Micro-strip ground plane is created by evaporating 2\( \mu \text{m} \) chrome-gold layer at the backside of the wafer. The fabricated structure along with RF connectors at the I/O ports is shown in Fig. 4. Thin film chip resistors are used as they offer minimal parasitics at higher frequencies and are mounted using conductive epoxy.
The performance parameters, measured, carried out using R&S ZVA-40 Vector Network Analyzer, are in close agreement with the simulation results as can be seen in Fig 5. The slight deviations are attributed to finite resistivity and its deviation from the assumed value. The maximum insertion loss achieved, with 8kΩ-cm resistivity wafer, of 6.8 dB can further be improved with higher resistive substrate. The input/output return losses better than 15 dB and isolation of 13 dB (min.) is achieved at two designed frequencies.

The performance parameters like insertion loss return loss and isolation indicates that silicon is a viable RF substrate and can be implemented as MIC substrate.

IV. CONCLUSION

This article reports the design of a dual-band power divider and realization on silicon substrate. Simulation study is carried out for glass and silicon media and measured performance for silicon realization are presented. The incorporation of the T-shaped SIR based stub is the novel feature of this topology. The design can be scaled to other frequencies, media and process implementations like MIC/MMIC. Further implanted resistors can be made with lead out CMOS process to avoid chip resistor and this process was successfully tried.

REFERENCES

[7] HFSS ver 10.5, Ansoft Corporation,